AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) An image processing system comprising:

synchronous type processing means for carrying out a first image process on image data that is the subject of processing;

asynchronous type processing means for carrying out a second image process on image data of a predetermined region of said image data that is the subject of processing; and

synthesize means for synthesizing an output of said synchronous type processing means and an output of said asynchronous type processing means to form one image data.

2. (Original) The image processing system according to claim 1, wherein said synthesize means comprises

a memory in which an output of said synchronous type processing means is stored, and

replacement means for replacing a portion of an output of said synchronous type processing means stored in said memory with an output of said asynchronous type processing means.

3. (Original) The image processing system according to claim 2, further comprising control means for controlling replacement timing by said replacement means by detecting status of an output of said synchronous type processing means stored in said memory.

4. (Currently Amended) An image processing system comprising:

a first image processor formed of a hardware circuit, and carrying out a first image process on input image data;

a second image processor carrying out a second image process on a [[portion]] fragment of said input image data according to a program of predetermined software; and

a memory in which image data subjected to said first image process and image data subjected to said second image process are synthesized and stored.

5. (Original) The image processing system according to claim 4, wherein data of said memory in which image data subjected to the first image process is stored is overwritten by image data subjected to the second image process.

6. (Original) The image processing system according to claim 5, wherein said second image processor detects a write timing of said image data subjected to the first image process into said memory to control a write timing into said memory.

7. (Original) The image processing system according to claim 4, wherein said software is rewritable.

8. (Original) The image processing system according to claim 4, wherein said second image processor detects a region on which the second image process is to be carried out by scanning input image data

9. (Currently Amended) An image processing method comprising the steps of:

carrying out a first image process on input image data through a hardware circuit;

carrying out a second image process on a [[portion]] fragment of the input image data through software; and

synthesizing image data subjected to the first image process with image data subjected to the second image process,

wherein sequence of said first and second image processes is arbitrary.

10. (Original) The image processing method according to claim 9, wherein said step of carrying out the second image process includes the step of detecting a region on which the second image process is to be carried out by scanning input image data, and carrying out the second image process on the detected region.

11. (New) An image processing system comprising:

a synchronous-type data processing device for carrying out a first image process on image data that is the subject of processing;

an asynchronous-type data processor for carrying out a second image process on image data of a predetermined region of said image data that is the subject of processing; and

a data synthesizing device for synthesizing an output of said synchronous-type processing device and an output of said asynchronous-type processor to thereby form one image data.

12. (New) The image processing system according to claim 11, wherein said synthesizing device includes:

a memory for storing and output of said synchronous-type processing device, and

wherein said synthesizing device replaces a portion of an output of said synchronous-type processing device stored in said memory with an output of said asynchronous-type processor.

13. (New) The image processing system according to claim 12, further comprising a controller for controlling a replacement timing in said synthesizing device by detecting a status of an output of said synchronous-type processing device which is stored in said memory.